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(54) Title: INSTRUCTION TIMING CONTROL WITHIN A DATA PROCESSING SYSTEM

(57) Abstract: A data processing system (2) is provided which is responsive to program instructions that operate in a variable timing mode to require a variable number of processing cycles to complete. The system is also operable in a fixed timing mode, which may be programmable using a bit (or several bits) within a configuration controlling register, to operate in a fixed timing mode in which such instructions are forced to operate using a fixed number of processing cycles. Thus, suppression of instructions which fail condition codes may be suppressed and early termination of program instructions similarly suppressed in a manner which helps resist an attack upon the security of the system by observing the number of processing cycles required to process certain data.